OIPE
JUL 18 2005
PATENT & TRADEMARK OFFICE 900

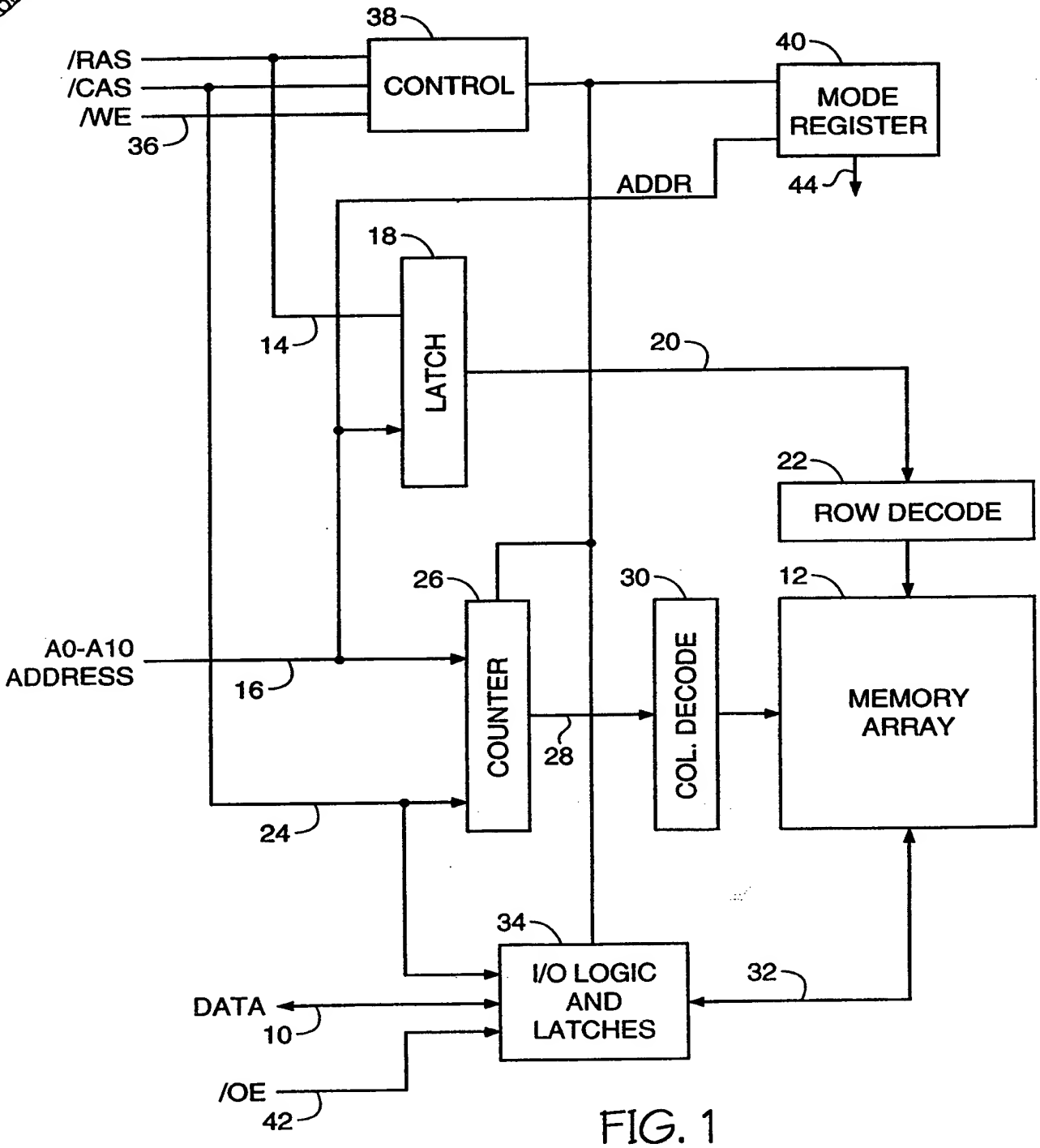

FIG. 1

Burst Length	Starting Column Address A_2	A_1	A_0	Linear	Interleave
2	V	V	0	0-1	0-1
	V	V	1	1-0	1-0
4	V	0	0	0-1-2-3	0-1-2-3
	V	0	1	1-2-3-0	1-0-3-2
	V	1	0	2-3-0-1	2-3-0-1
	V	1	1	3-0-1-2	3-2-1-0
8	0	0	0	0-1-2-3-4-5-6-7	0-1-2-3-4-5-6-7
	0	0	1	1-2-3-4-5-6-7-0	1-0-3-2-5-4-7-6
	0	1	0	2-3-4-5-6-7-0-1	2-3-0-1-6-7-4-5
	0	1	1	3-4-5-6-7-0-1-2	3-2-1-0-7-6-5-4
	1	0	0	4-5-6-7-0-1-2-3	4-5-6-7-0-1-2-3
	1	0	1	5-6-7-0-1-2-3-4	5-4-7-6-1-0-3-2
	1	1	0	6-7-0-1-2-3-4-5	6-7-4-5-2-3-0-1
	1	1	1	7-0-1-2-3-4-5-6	7-6-5-4-3-2-1-0

FIG. 2

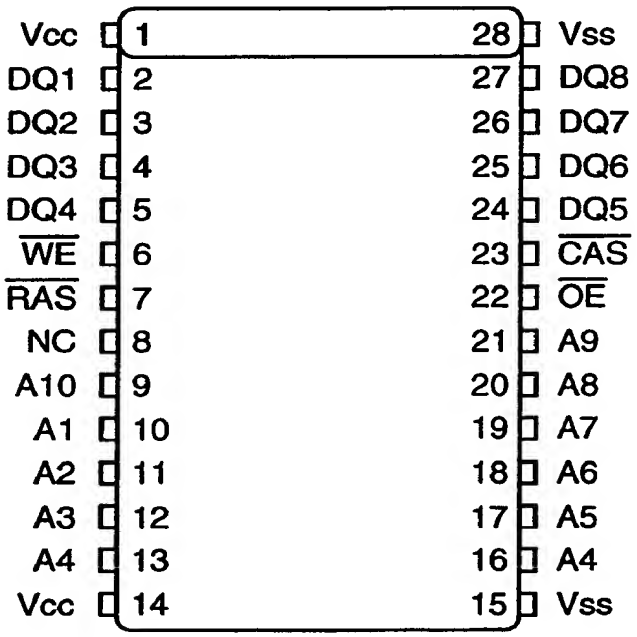
Vcc 1
DQ1 2
DQ2 3
DQ3 4
DQ4 5
WE 6
RAS 7
NC 8
A10 9
A1 10
A2 11
A3 12
A4 13
Vcc 14
28 Vss
27 DQ8
26 DQ7
25 DQ6
24 DQ5
23 CAS
22 OE
21 A9
20 A8
19 A7
18 A6
17 A5
16 A4
15 Vss

FIG. 3

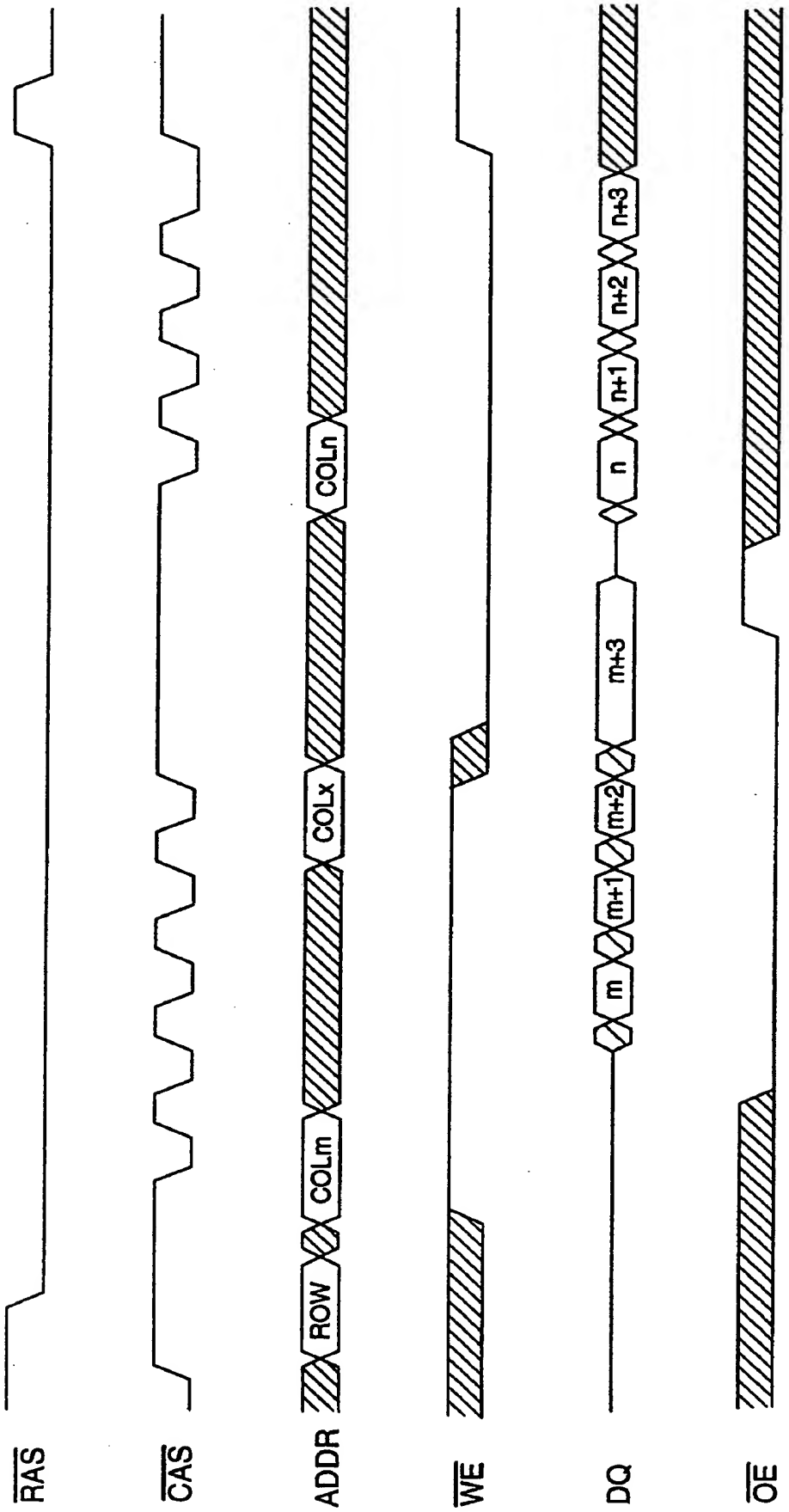

FIG. 4

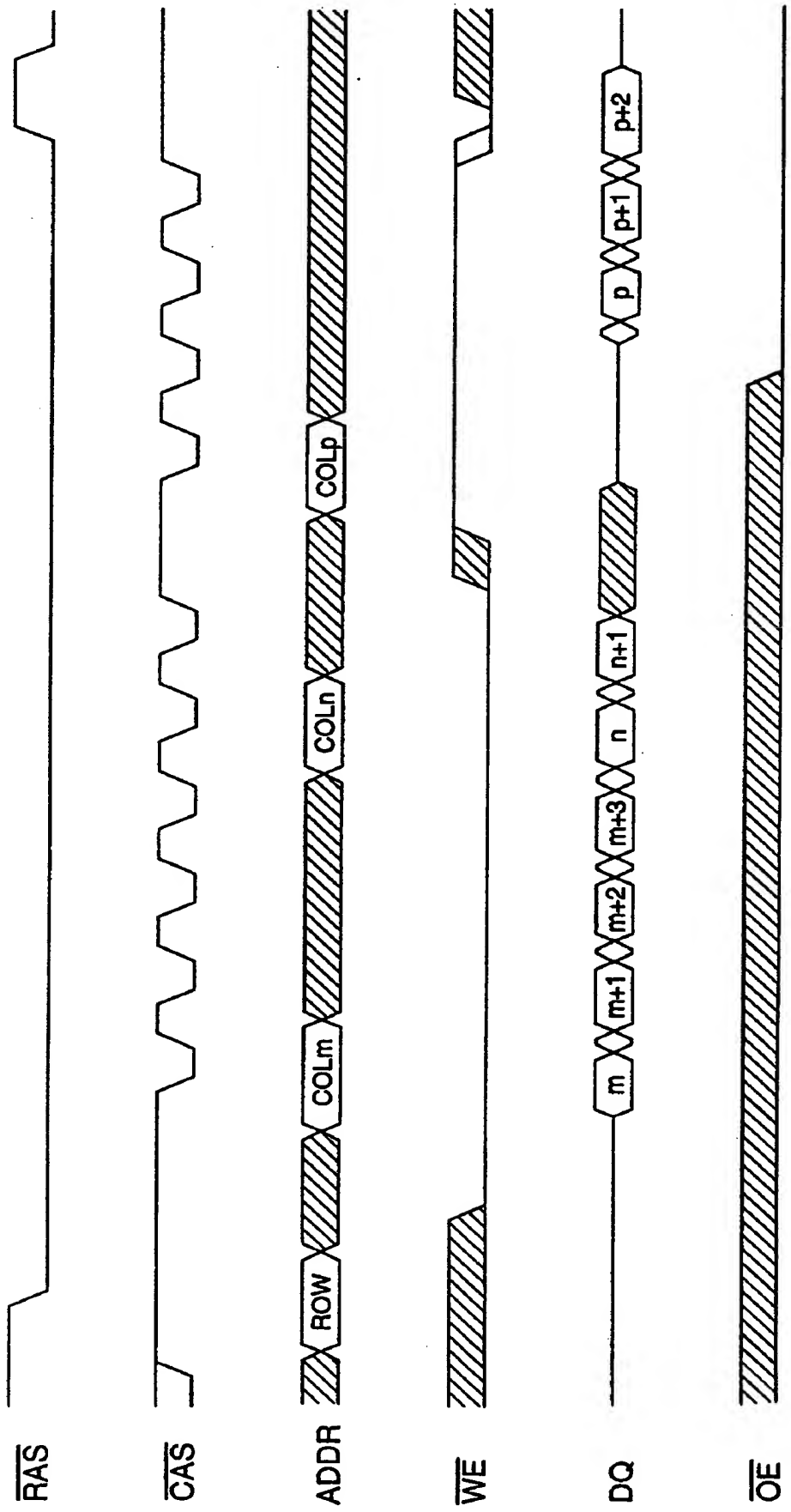

FIG. 5

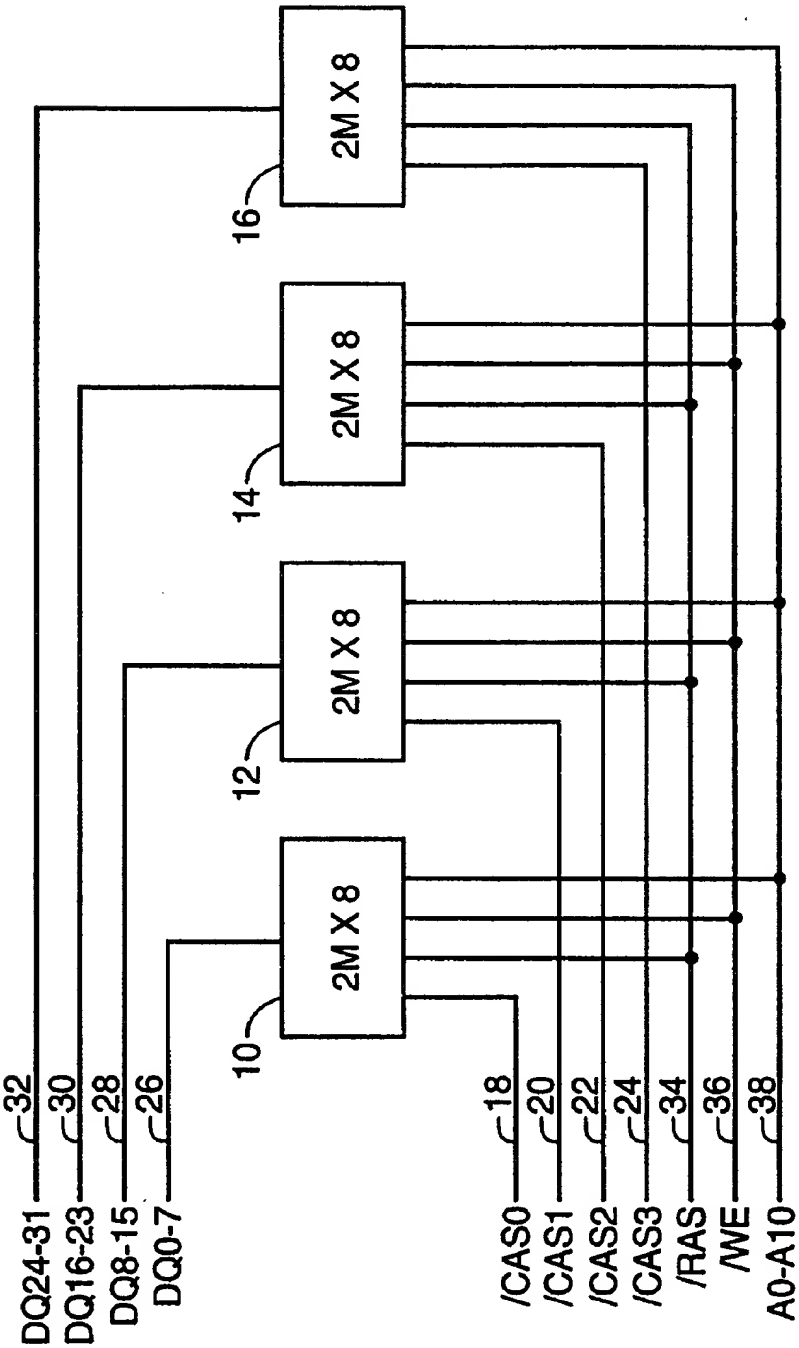
2M X 8
16
2M X 8
14
2M X 8
12
2M X 8
10
32
30
28
26
18
20
22
24
34
36
38
DQ24-31
DQ16-23
DQ8-15
DQ0-7
/CAS0
/CAS1
/CAS2
/CAS3
/RAS
/WE
A0-A10

FIG. 6

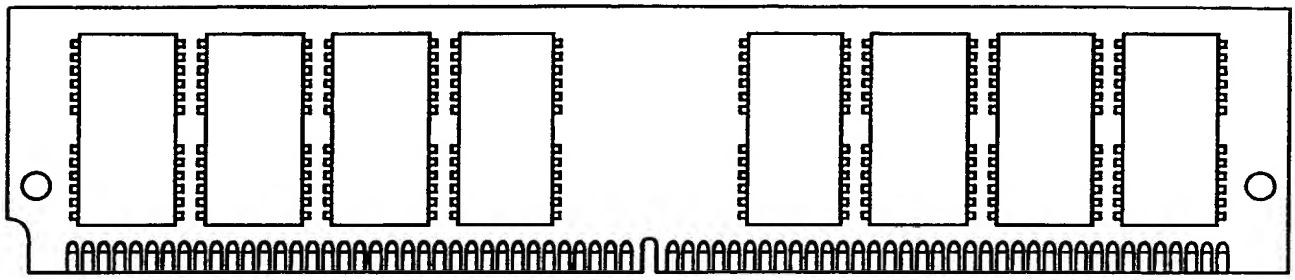

FIG. 7

PIN #	SYMBOL	PIN #	SYMBOL	PIN #	SYMBOL	PIN #	SYMBOL
1	Vss	19	A10	37	NC	55	DQ12
2	DQ1	20	DQ5	38	NC	56	DQ28
3	DQ17	21	DQ21	39	Vss	57	DQ13
4	DQ2	22	DQ6	40	$\overline{CAS0}$	58	DQ29
5	DQ18	23	DQ22	41	$\overline{CAS2}$	59	Vcc
6	DQ3	24	DQ7	42	$\overline{CAS3}$	60	DQ30
7	DQ19	25	DQ23	43	$\overline{CAS1}$	61	DQ14
8	DQ4	26	DQ8	44	$\overline{RAS0}$	62	DQ31
9	DQ20	27	DQ24	45	$\overline{RAS1}$	63	DQ15
10	Vcc	28	A7	46	$\overline{OE}$	64	DQ32
11	PD5	29	NC	47	$\overline{WE}$	65	DQ16
12	A0	30	Vcc	48	PD ECC	66	PD EDO
13	A1	31	A8	49	DQ9	67	PD1
14	A2	32	A9	50	DQ25	68	PD2
15	A3	33	NC	51	DQ10	69	PD3
16	A4	34	NC	52	DQ26	70	PD4
17	A5	35	NC	53	DQ11	71	PD refresh
18	A6	36	NC	54	DQ27	72	Vss

FIG. 8

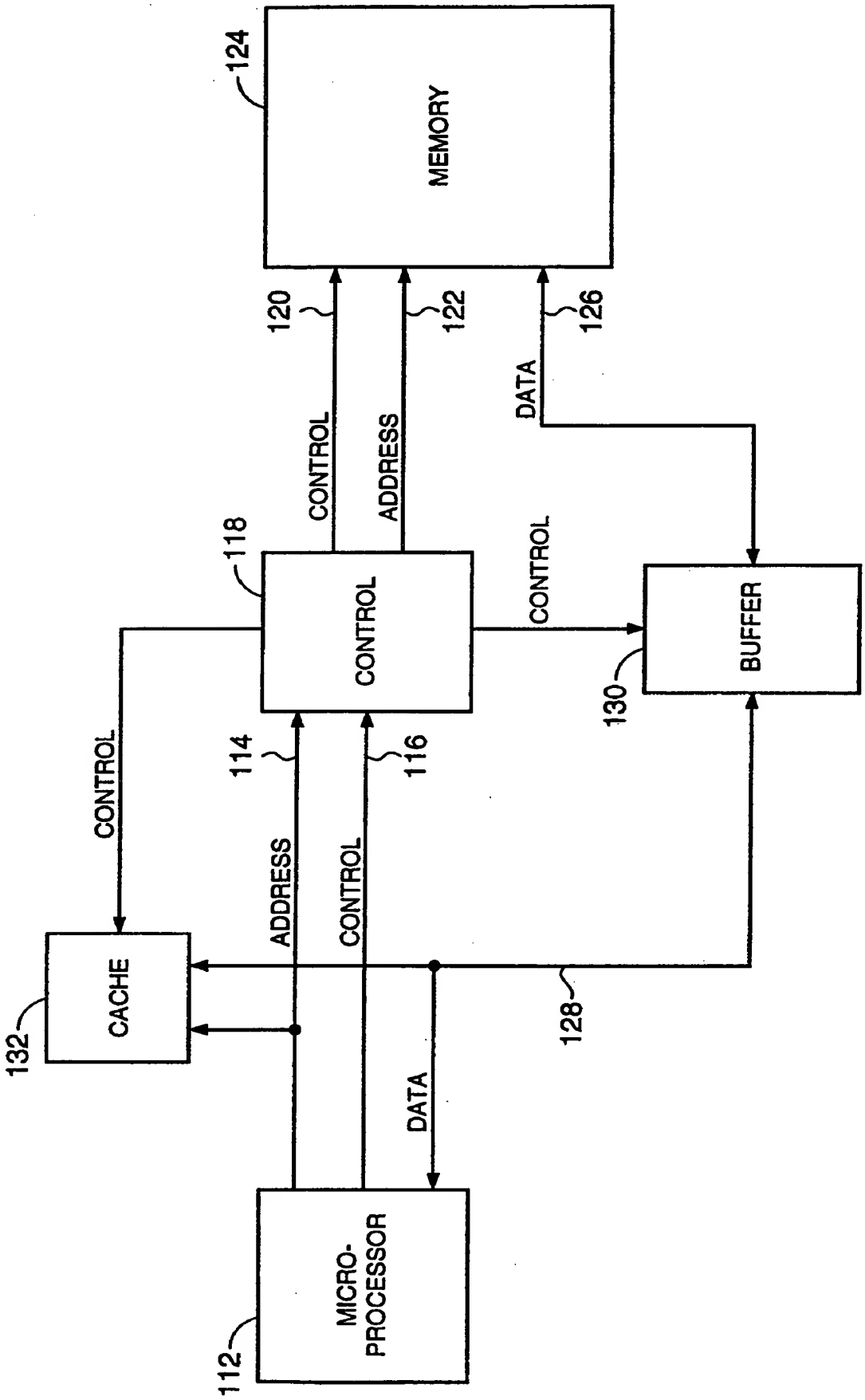
MEMORY
124
120
122
126
CONTROL
ADDRESS
DATA
118
CONTROL
CONTROL
BUFFER
130
CONTROL
114
116
ADDRESS
CONTROL
CACHE
132
128
DATA
MICRO-
PROCESSOR
112

FIG. 9

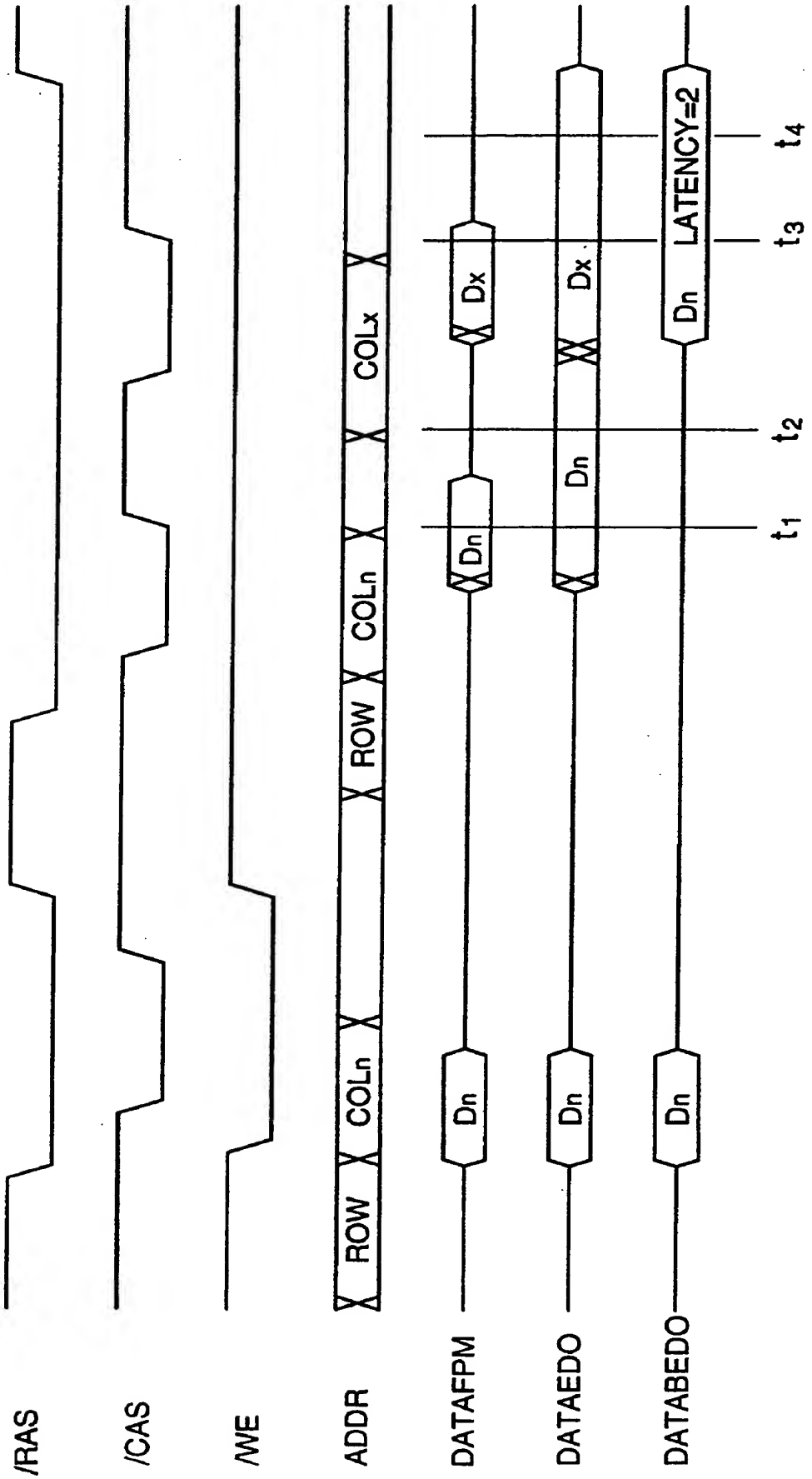
/RAS
/CAS
/WE
ADDR
DATAFPM
DATAEDO
DATABEDO
ROW
COLn
COLx
Dn
Dx
LATENCY=2
t1
t2
t3
t4

FIG. 10

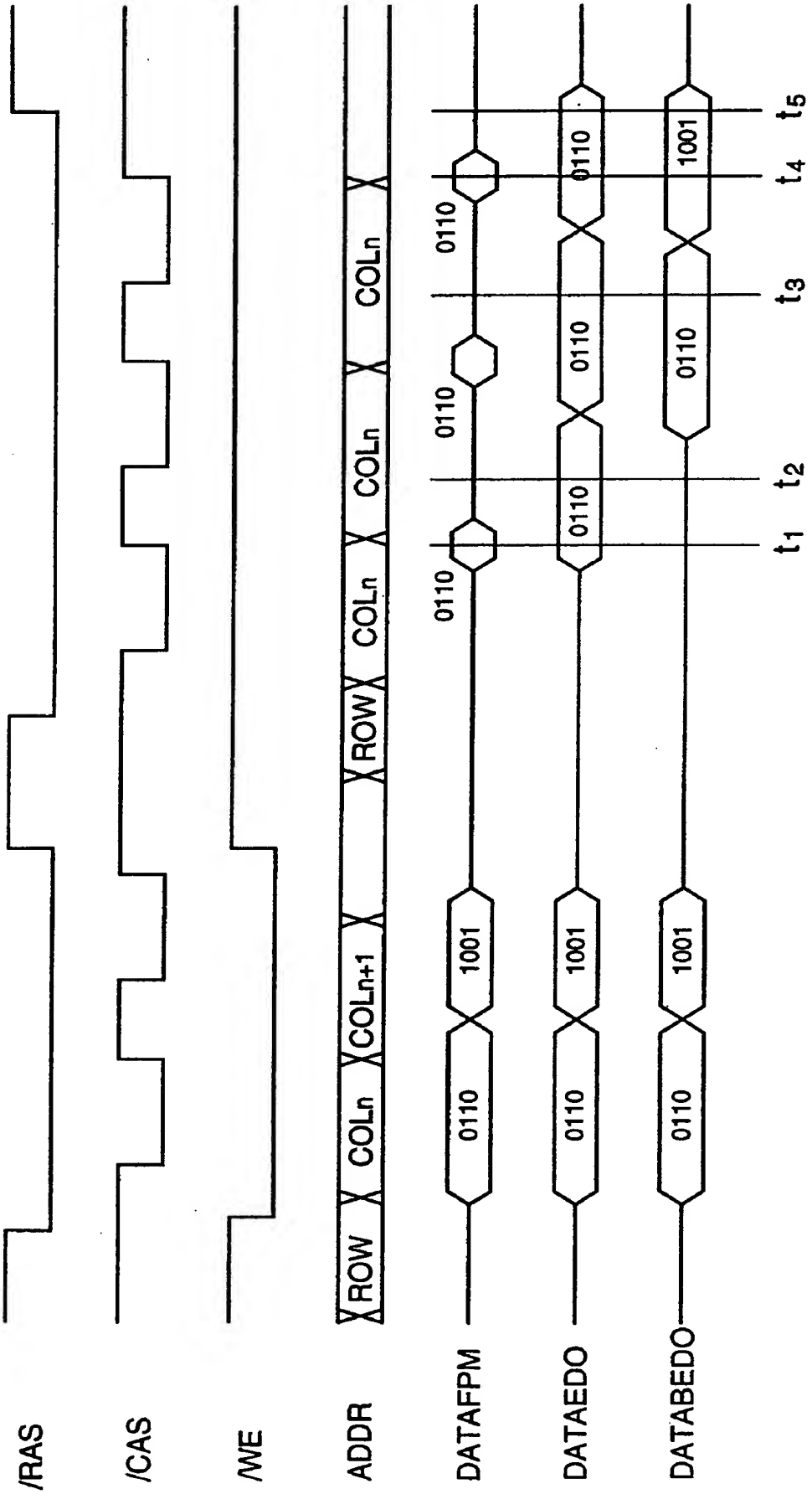
/RAS
/CAS
/WE
ADDR
DATAFPM
DATAEDO
DATABEDO
ROW
COLn
COLn+1
0110
1001
t1
t2
t3
t4
t5

FIG. 11